SDP Memo 55: Compute Node Hardware Technology Landscape Appraisal

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SDP Memo Disclaimer

The SDP memos are designed to allow the quick recording of investigations and research done by members of the SDP. They are also designed to raise questions about parts of the SDP design or SDP process. The contents of a memo may be the opinion of the author, not the whole of the SDP.

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List of Abbreviations

ARL .....Algorithm Reference Library
APU .....Accelerated Processing Unit
COTS .....Commodity off the Shelf
CPU.....Central Processing Unit
CUDA .....Compute Unified Device Architecture
EPYC.....a commercial brand not acronym
FFT.....Fast Fourier Transform
GB .....Giga Byte
GPU.....Graphics Processing Unit
HBM .....High Bandwidth Memory
HPSO .....High Priority Science Objectives
MSMFS .....Multi-Scale Multi-Frequency Synthesis
NVMe-oF.....Non-Volatile Memory Express over Fabrics
PCIe .....Periphery Connect Interface Express
ROCE.....RDMA over Converged Ethernet
RDMA.....Remote Direct Memory Access
SDP .....Science Data Processor
SKA .....Square Kilometre Array
SKAO .....SKA Project Office
SSD .....Solid State Disk
XEON .....a commercial brand not acronym

Introduction

- The term COTS is a frequently used but misused term. It projects the impression that it is a category of products that is non-differentiable from each other and is readily acquirable. SDP may well be constructed of COTS hardware but it is far from the truth that the resultant SDP system is also a COTS system. SDP has its own specific architectural traits and constraints. So, a SDP Memo for prescribing the way forward in hardware should justify being part of the documentation for CDR close-off.

- This Memo addresses the following issues without promoting any particular vendors. Such information will serve as a useful guideline during the Construction Phase leading to procurement of hardware.

  - What has SDP learned about COTS hardware in the last 12 months beyond the findings of an earlier report, a summary of which is included in an Appendix of this paper [APP1]?

  - How will the hardware landscape change from Element CDR (Q1 2019) until the deployment of the first SDPs several years later?

  - How accurate and believable are our scaling estimates?

  - What are the Technology Readiness Risks for mitigation if any?

References

Applicable documents

The following documents are applicable to the extent stated herein. In the event of conflict between the contents of the applicable documents and this document, **the applicable documents** shall take precedence.

[AD1] HPSO Requirements from SKA-TEL-SDP-0000038 SDP System Sizing

[AD2] Roofline an Insightful Visual Performance Model for Multicore Architectures, http://delivery.acm.org/10.1145/1500000/1498785/p65-williams.pdf

[AD3] SDP Memo 010: Estimating the SDP Computational Efficiency, Document number SKA-TEL-SDP-0000086 version C dated 2016-04-07

[AD4] SDP Memo 025: Updated SDP Cost Basis of Estimate June 2016, Document number SKA-TEL-SDP-0000091 version C dated 2016-06-06

[AD5] SKA-TEL-SDP-0000094 Updated SDP Cost Basis of Estimate Sept 2016

[AD6] SDP Cost Basis of Estimate update Feb 2017, Document number SKA-TEL-SDP-0000108

[AD7] SKA-TEL-SDP-0000038 System Sizing

[AD8] Scalability, Cornell University Centre for Advanced Computing, *https://www.cac.cornell.edu/education/training/StampedeJan2015/Scalability.pdf*

[AD9] SDP Memo 54: Compute Node Pipeline Compute Efficiency Assessment Framework

[AD10] Technology Readiness Assessment Guide, DOE G 413.3-4A, 9-15-2011 http://www2.lbl.gov/dir/assets/docs/TRL%20guide.pdf

Reference documents

The following documents are referenced in this document. In the event of conflict between the contents of the referenced documents and this document, **this document** shall take precedence.

[RD1] Generative Adversarial Networks recover features in astrophysical images of galaxies beyond the deconvolution limit, ETH Zurich, arXiv:1702.00403v1 [astro-ph.IM] 1 Feb 2017

[RD2] PSFGAN: a generative adversarial network system for separating quasar point sources and host galaxy light. arXiv:1803.08925v1 [astro-ph.GA] 23 Mar 2018

[RD3] Identifying Exoplanets with Deep Learning: A Five Planet Resonant Chain around Kepler-80 and an Eighth planet around Kepler-90, Google Brain and U Texas, 2018-07

1 Compute Node Hardware Landscape

1.1 Recent Findings

What has SDP learned about COTS hardware in the last 12 months beyond the findings of an earlier report, a summary of which is included in [APP1] of this paper? Investigation findings and observations are collected below.

– Processors
– Non-Processors

Processors

a) Memory installed in a compute node is confirmed to be the primary constraint for SDP as the dimensions of visibility grids and images are totally dependent on memory available [APP2]. For example, 64GB of main memory can only handle a grid shape of [8,1,8192,8192] and doubling of grid size leads to 4 times of memory. Unfortunately, memory prices have stayed high at unprecedented levels in recent years due to high demands from an ever expanding array of big data applications.

b) Memory bandwidth is the second constraint due to the sheer scale of SDP data flow. It impacts on the ceiling of peak hardware compute capacity of devices available to science pipelines or applications as prescribed by the Roofline Model [AD2]. The resultant ceiling is known as the Roofline Efficiency [AD3]. As Compute Efficiency is the product of Roofline Efficiency and Programming Efficiency [AD9], it has a direct impact on Compute Efficiency. Additionally it impacts on the scale of distributed computing as a component of the overhead cost of distribution [AD4].

c) Compute capacity is the third constraint but it has been treated as the key parameter for SDP system sizing. Irrespectively compute capacity is vital for reducing SDP scalability concerns.

d) GPU has a computational capacity many times of CPU and it is considered the most viable device type for providing most of the compute resources. However, the x86 Acceleration Model that provides for GPU kernel operation requires the CPU to be the host processor and therefore CPU is needed for SDP. The CPU handles I/O and the sequential portion of application.

e) Range of CPU on the landscape

- CPUs are referred by SDP as “latency optimised cores optimised for latency sensitive operations, such as receiving large volumes of streaming data and real-time processing of that data. Generally these are large superscalar, out-of-order cores with multiple stages of cache, found in mainstream products from Intel, IBM, AMD and various ARM licensees.” This is done to be as technology agnostic as possible.

- In addition to the above mentioned standard features, the following factors affect latency, service time, service request rates, and scaling abilities which are relevant

issues for SDP. These other factors are the differences between RISC and CISC, SIMD engine provisions, operating frequencies, and amount of cache per core.

- Xeon has always been considered as the default server processor due to its market dominance. However, the latest range which Intel marketed as Xeon Scalable Processors is significantly more expensive than competing products at the high end of the range.

- Single Socketed EPYC processors from AMD offer special appeals in having 8 channels of DDR4 memory and 128 PCIe lanes. The memory bandwidth and memory real estate installable are favourable to SDP requirements. Since SDP need more GPU compute capacity than CPU, having a single socket supporting 2 or more GPU devices appeals to SDP.

- ARM processors called ThunderX2 designed by Cavium have been installed in Sandia National Lab in USA. However, the processor was reported by a media source to be 25% inferior to Intel Xeon in performance. https://www.nextplatform.com/2018/06/18/sandia-lends-arm-a-hand-with-astra-supercomputer/

- IBM Power9 + Nvlink + OpenCapi would technologically be very interesting. However, currently systems are prohibitively costly.

f) APU implementing the Heterogeneous System Architecture has appeals to SDP due to the immediate vicinity of the integrated GPU cores to the CPU skipping the standard PCIe connections for discrete GPU. Unfortunately, the vendor AMD has not implemented mature computing drivers to the devices currently available (as tested in 2018-07) and test results were inconsistent to be considered reliable [APP4].

g) GPU. Owing to the development of GPU cards tightly with CUDA libraries, Nvidia GPU cards can have higher performance than AMD GPU cards which are OpenCL compliant. This situation is understandable, and AMD has proceeded to develop its ecosystem ROCm (for Radeon Open Compute Platform) which is analogous to CUDA so that AMD GPU cards will have dedicated libraries for optimal performance. ROCm reached v1.8.2 and is functional for discrete Vega GPU devices. How close ROCm is to OpenCL is an issue being monitored and considered for SDP adoption.

h) HBM has been available on high-end GPU cards for a couple of years and it helps to reduce the operational intensity of the ridge point of the GPU device to a lower level. This helps to raise the 'Roofline Efficiency' [AD2] accessible by applications. However, HBM attracts high price and its availability has been limited.

Other Hardware Devices

i) Intel Optane has been available as SSD on PCIe since 2017. Intel has planned to release Optane as Non-Volatile DIMM persistent memory (NVDIMM) in the second half of 2018. This NVDIMM will have 4 times the density of DDR4 in GB per module and it will create a new category of hot buffer. SDP shall take note of this technology.

j) NVMe-oF and ROCE have the potential to reduce the latency of inter-node data transfer and improve throughput.

k) 25GbE/50GbE Ethernet Switches experienced the biggest drop in price over the last 12 months. An industry observer stated that they dropped as much as 40% in a year. https://www.nextplatform.com/2018/06/08/the-old-switcheroo/.

1.2 Hardware Landscape Trends

How will the hardware landscape change from CDR until the deployment of the first SDPs? Has Moore's Law continued or ceased to influence the landscape, see [APP3]? This section deals with developments that affect computer hardware size, performance, wattage and price in a 5 year near term timeframe.

- Semiconductors
- Inter-Processor Links
- Potential of FPGA
- Virtualization

Semiconductors

a) Moore's Law has prescribed the development of semiconductor fabrication techniques for the last 50 years. As Gordon Moore is the prescriber of the law and a founding director of Intel, Intel's performance is taken as the indicator of the validity of the law. Moore's Law has now hit the wall as Intel has taken 4 years at present (2018-07) instead of 2 years prior to 2015 to evolve its processors to the next generation. The latest range of Intel Scalable Processors is fabricated on 14nm process which is in its 4th year in Intel. Process length is important because it affects the density of logic gates that can be packed in a given area which in turn relates to computing performance and operating wattage. The significant price premium that Intel assigned to the current range also indicates the relationship of process length with price. It is well known in the semiconductor industry that the cost of taping out a new design goes up exponentially as the process length gets small.

    - Intel has announced the delay of releasing 10nm desktop processors (labelled Cannon Lake) to 2019 claiming that its goal of 2.7x logic density over 14nm was ambitious thus needing more time. Intel also claimed that it has achieved 70% performance gain over the 4 years on 14nm and so the waiting time was not wasted. https://www.anandtech.com/show/12693/intel-delays-mass-production-of-10-nm-cpus-to-2019. SDP can expect 10nm server processors to be available before 2023.

b) Taiwan Semiconductor Manufacturing Company (TSMC) is the biggest open foundry in the world. In 2016, TSMC moved its 10nm process to volume production, and completed the validation of its 7nm technology. Compared to its 10nm process, 7nm features 1.7x logic density for ~30% speed improvement or ~60% power reduction. https://www.anandtech.com/show/12677/tsmc-kicks-off-volume-production-of-7nm-chips

- Observers have commented that TSMC 7nm is roughly similar to Intel 10nm and so the figures of 30% speed improvement or 60% power reduction is what SDP can expect by 2023.

c) Applied Materials which supplies semiconductor materials to foundries has found new materials that would allow semiconductor fabrication process length to hit 5nm and below. https://www.eetimes.com/document.asp?doc_id=1333471

Inter-Processor Links

d) Current processors from Intel, AMD and Nvidia are reliant on the PCIe v3 standard for inter-processor communication within the compute node. However none of them have moved to PCIv4 yet. It was IBM which first released PCIev4 in its Power9 systems in 2017. PCIe v4 is double of the bandwidth of v3 to reach 32GB/s for one direction over 16 lanes. It will surely help reduce the cost of data transfer between the CPU and GPU for SDP applications when Intel, AMD, and Nvidia make it available in their products.

e) Intel has announced PCIev4 for its 10nm Cannon Lake desktop processor and for its Falcon Maser 10nm FPGA card. https://www.tomshardware.co.uk/intel-ai-10nm-pcie-4.0-wafer,news-56785.html

f) AMD has not made any announcement on PCIev4. Instead rumours have turned up that AMD may skip v4 and go straight to v5 which is double the bandwidth of v4 to hit 64GB/s for one direction over 16 lanes. PCI SIG is the body maintaining the PCIe standard. It has scheduled PCIev5 to be ready in 2019. https://techreport.com/news/32064/pcie-4-0-specification-finally-out-with-16-gt-s-on-tap

g) OpenCAPI v2, CCIX, and GEN-Z are other inter-processor links available or in the works. OpenCAPI is closely related to IBM and CCIX is closely related to ARM. Their chance of being adopted by COTS vendors is low. On the other hand, Intel is not a member of GENZ consortium and this situation will affect the uptake of GEN-Z.

h) GEN-Z takes the memory controller and PCIe controller out of the CPU die and treats CPU, GPU and all devices in the compute node as peers as far as data communication is concerned. FPGA, SOC, and any computing devices are treated the same as the CPU or GPU. It also takes the wall out from separating addressable memory modules and block storage devices. https://genzconsortium.org/wp-content/uploads/2017/08/Gen-Z-Overview.pdf. SDP will surely benefit from GEN-Z when it is available.

- The mechanical design of GEN-Z slots is similar to PCIe slots, whereas the data transfer rates vary between 50GB/s to 448GB/s. The first version of GEN-Z will be ready by the end of 2019. SDP should be in time to enjoy its benefits.

Potential of FPGA

i) FPGA is the chosen technology for CSP Correlators. Would FPGA have any appeals to SDP over time? Intel has announced Falcon Maser PCIe FPGA card for 2019 release. Would this event trigger the commoditization of FPGA for x86 systems?

j) SDP involves algorithms that are likely to make advancements over time. The current SDP Algorithm Reference Library is written in Python for ease of coding and documentation, whereas C and OpenCL are the highest level of programming language available for FPGA today. OpenCL for FPGA programming is not yet popular as it is highly dependent on the FPGA vendor to provide the compiler to produce the code that can be placed and timed.

k) Data streaming is one application type that FPGA would excel as FPGA is capable of providing multiple steps of processing within the same die. GPU cannot do the same economically. GPU does not allow logic flow to be spatially laid out like FPGA to allow input data to stream through to the end of the pipe with the entire pipe fully populated.

Virtualization

l) SDP has been exploring the use of containers for compute node and the use of scheduler for separating work flow control from compute logics. Both efforts are aimed at flexibility and abstraction of hardware. They are an inevitable step of technology evolution. However, how would hardware assist in this evolution process?

m) There are 3 streams of software driven efforts for virtualisation. They are Software Defined Computing, Software Defined Storage and Software Defined Networking. Apart from offering user friendliness and flexibility, they will all cause lowering of the cost of hardware. This memo is focussed on computing and has not looked into storage or networking.

    - MVAPICH2 announced its Virt-2.2 edition to support Docker and Singularity containers. This is obviously good news for the HPC domain. https://insidehpc.com/2018/04/exploiting-hpc-technologies-accelerating-big-data-processing-associated-deep-learning/

n) On the flip side, there is a hardware compute cost for all types of software abstraction. For example, running containers in a compute node would cost one CPU core, which is the minimum unit assignable with software, and its share of main memory. Exactly how much is the cost will depend on various scenarios which are subject for benchmarking when the SDP architecture is more firm. The biggest threat to compute node is in scaling and virtualisation may deepen the threat.

1.3 SDP Size Estimates

How accurate and believable are our scaling estimates? What is the certainty that SDP will be built hardware-wise to deliver its pre-defined HPSO requirements [AD1] within budgetary and wattage constraints on the technology side if not on the financial side?

- Global Statistics in 2018
- Projections to SDP System Size Target

Global Statistics in 2018

a) Summit Supercomputer at Oak Ridge National Laboratory of USA was ranked the first position on the TOP500 High Performance LINPACK (HPL) list in 2018-06. The statistics of Summit relevant to this paper are listed below. It can be seen that Summit has a high compute efficiency (122.3 / 200 = 61.15%) and a high power efficiency (13.9 GFLOPs/watt). To put the figures into perspective, SDP was previously estimated to need a Raw Peak of 259 PFLOPs DP and a compute efficiency of 10%.

   Raw Peak: 200 PFLOPs DP
   HPL Score: 122 PFLOPs DP
   Power Efficiency: 13.9 GFLOPs DP per watt (5th GREEN500)
   CPU: IBM 9,216 Power9
   GPU: NV 27,648 V100 via NVLINK
   Wattage: 13MW

b) TOP500 has a High Performance Conjugate Gradient (HPCG) list which is intended to be a complement of the HPL list. Whilst HPL emphasises high compute rate, HPCG emphasises high memory transfer rate. Summit was ranked first on this HPCG list (as well as the HPL list) with a score of 2.925 PFLOPs which is 2.4% of HPL score. https://www.top500.org/hpcg/lists/2018/06/. SDP applications have compute properties that fall in both categories, for example, FFT is closer to HPCG and MSMFS is closer to HPL.

c) Power Efficiency: The top system achieved 18.4 GFLOPs/watt during its 858 TFLOPs Linpack performance run. The figure dropped to 10.4 for the system ranked number 10. https://www.top500.org/green500/ & https://www.top500.org/static/media/uploads/top500_ppt_201806.pdf. SDP should aim for Top 10 or higher.

Projection to SDP System Size Target

d) SDP processor platform hardware requirements were last stated [AD4] as shown in the table below based on an overall SDP Compute Efficiency of 10% [AD5]. The hardware figures have since survived 2 subsequent rounds of Cost Estimation in 2016-09 [AD5] and 2017-02 [AD6].

Processor Platform			
Compute	**Low**	**Mid**	**Units**
Number of nodes	896	786	
GPUs Per Node	2	2	
Peak Performance per GPU est.	31	31	DP TFlops
Memory per Node	320	512	GB
Storage per Node	See Below	See Below	
BDN Connection per Node	25 GbE	25GbE	GbE
LLN Connection per Node	56Gbps/50GbE	56Gbps/50GbE	
DPN Connection per Node	10	10	GbE
Number of compute islands (CI)	16	15	
Nodes per compute island	56	56	

e) The document [AD6] dated 2017-02 Section 6.1 System Sizing has the following comments: "We use a model schedule to estimate the average load and estimate the system size based on an averaged processing load over a two week period - this approach is consistent with the previous cost submission and is described in SKA-TEL-SDP-0000094 Updated SDP Cost Basis of Estimate Sept 2016 (which is [AD5] of this paper)".

f) According to the table (based on the average approach), the total peak capacity to be installed for LOW is 55.552 PFLOPs DP and for MID is 48.732 PFLOPs DP. The 'average approach' total is 104.3 PFLOPs DP.

g) The same document [AD6] dated 2017-02 Section 6.1 System Sizing also has this following statement, "As for the September 2016 submission, our sustained computational performance required is 13.8 PFLOPs for LOW and 12.1 PFLOPs for MID". This statement referred to 'sustained' versus 'average approach' above. The sustained total load is 25.9 PFLOPs.

h) There are 2 system sizing figures for addressing- one is 104.3 PFLOPs DP from an average approach based on 10% compute efficiency and the other is 25.9 PFLOPs DP of sustained loading. To put the 2 figures on the same footing, the target system size based on sustained load and 10% compute efficiency would be 259 PFLOPs DP. For risk analysis purposes, 259 PFLOPs DP shall be the target.

i) This SDP target is slightly higher than Summit's 200 PFLOPs DP. Assume that SDP hardware supply tendering starts in 2023. Based on the information in Section 3.2 Semiconductors, chances are very high that the SDP target would be met easily by the industry. Besides, a recent SDP compute node study [APP5] has indicated that 10% is too pessimistic for SDP compute efficiency. Another SDP study has suggested that Single Precision is acceptable to SDP pipeline calculations- if accepted, it will further reduce the SDP system size target. The picture is positive although it is more intuitive than evidence based. It is necessary to repeat this study annually.

1.4 Long Term Perspective of Hardware

How would the initial SDP hardware system influence or impact its evolvements for the next 50 years of lifetime? This issue refers to the strategy of hardware replacement cycles in order to optimize the benefits of upcoming technologies without causing programming disruptions of a significant scale that would affect SDP operations and maintenance. This section deals with evolutions of macro-architecture beyond the next 5 years of a speculative nature. Not only revolutionary hardware will appear on the horizon, the corresponding programming model will change as well. Therefore SDP shall not see the initial system as the only way to go and shall be vigilant of upcoming technologies and get prepared.

- In-Memory Computing
- Machine Learning
- Quantum Computing

In-Memory Computing

a) Assume *(A)* denotes information stored in a memory location. To perform a computational operation *f on (A)* and to store the result in the same memory location, data is shuttled to and back between the memory and the processing unit in competition with the instruction for transfer. This is not desirable and is known as the Von Neumann Bottleneck.

b) An alternative architecture is where *f* (*A*) is performed in place in the same memory location. One way to realize computational memory is by relying on the state dynamics of a large collection of memristive devices. Depending on the operation to be performed, a suitable electrical signal is applied to the memory devices. The conductance of the devices evolves in accordance with the electrical input, and the result of the operation can be retrieved by reading the conductance at an appropriate time instance. Nature Communications 8, Article number: 1115 (2017) doi:10.1038/s41467-017-01481-9 (open access)

c) Interconnected by high-bandwidth silicon photonics, Intel is able to "disaggregate" processing, memory, storage and acceleration onto modules called "sleds". This enables a completely homogeneous hardware design for data centres which can be completely software-defined on very small scales without human intervention. https://seekingalpha.com/article/4142794-intels-secret-industrial-scale-data-center-architecture?

d) IBM's answer to this challenge is an analogue phase-change memory (PCM) chip. IBM's PCM unit would serve as a CPU accelerator. This technology would substantially improve compute efficiency and energy efficiency if successful. https://www.zdnet.com/article/ibm-our-in-memory-computing-breakthrough-will-cut-cost-of-training-ai/

Machine Learning

e) Machine Learning is being developed on both the algorithm and hardware fronts. Algorithm refers to the replacement of the current style of domain expert rule-based programming with finding patterns from big data. Hardware refers to physical devices

that operation on low precisions such as 16 bits down to 1 bit for inferencing. There are already academic papers published [RD1] [RD2] [RD3] on the success of the algorithm approach in astronomy imaging. It is likely that Machine Learning algorithms have an increasing role to play in SDP in the near future.

Quantum Computing

f) Quantum computing is the ultimate in parallel computing. It may be able to simulate more phenomena in nature to advance research. Whilst many countries are investing in hardware research and development, USA Oak Ridge National Laboratory has released simulation facilities to scientists to get a feel of this new computing regime. XACC is a compiler developed at Oak Ridge for providing abstraction of hardware for application programmers. It is based on C++ but programmers need to understand quantum physics to appreciate how gates work. How many programmers for astronomy applications understand quantum physics? A lot of astronomers are familiar with quantum physics.

g) Operation is currently performed under extreme low-temperature, high magnetic field, and in a vacuum or sterile environment, making the technology extremely difficult to scale and expensive to operate. It is therefore not surprising that quantum computing is unlikely to achieve the distribution level of classical computers anytime within the next 10 years. Source: ABI Research published via Digitimes on 2018-07-24. https://www.digitimes.com/news/a20180724PR202.html?mod=2

2 Technology Readiness Risk Assessment

- What is the current Technology Readiness Level (TRL) if SDP Construction Tenders are issued tomorrow? What are the risks? What are the potential trade-offs for consideration?

- SDP has adopted the Scaled Agile Framework (SAFe) for project management. Does SDP need another framework such as TRL? SAFe is a framework of techniques for software development projects. It describes the roles, responsibilities, artefacts, and activities necessary to implement a project. On the other hand, TRL focuses on technology readiness and does not provide techniques for managing resources. It is useful as an indication of the gaps to be filled for the completion of the project for real life deployment.

2.1 Hardware Technology Level Assessment

a) Technology Readiness Assessment is a systematic metrics-based process that assesses the maturity and risks of critical technologies to be developed in a project. A lot of guidelines can be obtained from the Department of Energy in USA as they have funded the construction and operation of many supercomputer centres.

b) As SKA plans to build Low SDP and Mid SDP with COTS hardware, SKA obtains the benefits of free crowd-source testing and validation services for COTS hardware. As far as hardware technology assessment is concerned, SKA needs to attend to how different SDP is to other supercomputers. Most if not all supercomputers ranked on the TOP500 HPL list were built for HPC purposes. How much cloud computing features do they possess? Is SKA going to build the two SDP with HPC features, cloud features, or a mix of them? This is a software consideration as well as a hardware consideration.

c) On the hardware side, the performance and power efficiency of executing SDP science pipelines is yet to be tested.

d) The USA DOE TRL Assessment Guide [AD10] defined 9 levels of deployment readiness from 1 for preliminary investigation to 9 for completely ready. For intuitive assessment of confidence on technologies, there is a simpler and smaller framework as shown below. This paper attempted to place the current SDP status onto this intuitive framework.

   - TRL3 Low fidelity of the behaviour of the complete system
   - TRL4 Medium fidelity
   - TRL5 High fidelity
   - TRL6 Complete fidelity and Ready to Manufacture

e) Supply of Required COTS Hardware would be on TRL4 for Medium Fidelity at present and the natural progression of the supply industry would take SDP to TRL5 and TRL6 within the next 5 years before SKA places tenders for hardware supply.

f) Performance & Power Efficiency would be on TRL4 at present based on proven and effective efforts of performance optimisation for science algorithms by the Oxford team [APP 5] and the establishment of a compute efficiency measuring framework by New Zealand Alliance [SDP Memo 54].

g) Compute Cluster Scaling would be on TRL3 at most. Previous tests done by Tim Cornwell [APP6] indicated the presence of sub-linear scaling and tests in progress in NZA at the time of this draft (2018-08) indicated the existence of a serious issue for investigation.

h) System integration of SDP hardware with science pipelines and middleware would be on TRL3 as down-selection of middleware candidates has yet to happen and the efforts of prototyping pipelines to demonstrate they work within the Execution Control component were at an exploratory stage by 2018-07. https://confluence.ska-sdp.org/display/WBS/SIP+Sprint+11%3A+2018D

2.2 Potential Risks

a) The following areas of major risk have been identified for achieving the performance target.
   - Memory real estate and bandwidth
   - Compute Cluster Scaling to achieve performance
   - System integration with middleware for science pipeline execution to achieve performance

b) The availability of memory real estate and bandwidth is a pure hardware and price issue. As far as the CPU supply landscape is concerned, AMD EYPC provides the best contemporary offer in terms of performance and price for a memory bandwidth based on 8 channels of DDR4, and a maximum of 2TB supportable per socket or 4TB per dual-socket node. More memory and high bandwidth are desirable and never enough for most HPC systems including SDP. The supply industry will likely achieve doubling of the capacity of each feature over the next 4 to 5 years. The same rationale applies to GPU as a category. Nvidia V100 GPU provides the best contemporary offer in terms of performance with 32GB of HBM2 memory and 900GB/s of theoretical bandwidth. https://www.anandtech.com/show/12576/nvidia-bumps-all-tesla-v100-models-to-32gb

c) Compute cluster scaling depends on both hardware and software factors. Hardware factors include operating frequency, cache size, memory size, memory bandwidth, PCIe bandwidth, and inter-node connectivity bandwidth. As mentioned above, the supply industry will likely achieve doubling of each criterion over 4 to 5 years. On the software side, factors include science algorithm logic, its programming language, data partitioning patterns, and the scheduler.

d) System integration is mostly dominated by software factors assuming that hardware factors have been addressed above.

2.3 Potential Trade-offs

a) The following dimensions of architectural features have been identified as the dials of trade-off for risk mitigation. The first factor is hardware. The second factor is software versus hardware.

   - COTS versus Proprietary Hardware
   - Flexibility versus Performance

b) Proprietary hardware in fact includes software. CUDA based GPU devices are a good example. CUDA is a software API or collection of libraries. CUDA based GPU were tightly tied to the API and libraries for optimal performance. On the other hand, OpenCL is an open standard and it is applicable to more than one hardware vendor. Science pipeline applications are therefore portable if written with OpenCL API. However, individual vendors would find it harder to optimise hardware to an open standard since the open standard could not be trimmed to match the hardware. CUDA based GPU would run OpenCL-based applications but OpenCL was not the basis of design of CUDA hardware. Ref: https://www.researchgate.net/post/Could_you_tell_me_how_to_run_OpenCL_programs_on_Nvidia_GPUs

c) Flexibility refers to programming, portability, and system design. Higher flexibility gives lower performance as there is a cost that reduces performance. Flexibility is desirable and SDP will need to do some sort of trade-offs eventually. Below are three examples for illustration purposes. There are further abstraction opportunities such as in the choice of middleware.

   - Take Python- a high level interpreter language as an example. It is highly popular among science research communities for its scripting simplicity. On the other hand, C based programs take a lot less time than python programs to execute but it is harder to program. It is a case of programming time versus runtime.

   - Containers provide an isolated and complete operating environment for applications developed with the same container. Moving containers around is easier than moving naked applications around. However, containers incur a cost of abstraction. Each container consumes some CPU time and memory real estate.

   - In terms of system design, the issue of work flow scheduling is a good example. One extreme case of work flow is if all process components were assigned to the same compute node for execution instead of dynamically allocated to various nodes available. If memory is a big issue, then the single node arrangement will run a lot faster.

2.4 SAFe for TRL

a) The concept of agile development is applicable to SDP Hardware and Compute Node technology readiness assessment. This memo has captured key factors and key developments for attention as at 2018-08. Similar efforts of an iterative agile nature shall be repeated in 2019 and 2020 to reach TRL6 well before supply tenders for hardware are issued. This will allow time for SDP to reach TRL9 on schedule and for new ideas to be developed for the benefits of the next 50 years of SDP operation.

b) Specific technologies to watch include the adoption of PCIev4 or GEN-Z for x86 hardware vendors. Either will lift the playing field and will be a desirable feature for SDP to have. Hopefully, this will happen in 2020.

c) The slowdown of Moore's Law is not a threat to SDP even after its total demise. Architectural innovations are the new emphasis and they could be more powerful than Moore's Law. In-memory computing would be a new technology having the highest level of positive impact on SDP. Its maturity is estimated to be more than 5 years away.

d) Some technology down-selections by SDP in the immediate future would help. With the reduction of scope for deeper analysis, the context will swiftly shift from "can SDP be built for the pre-defined budgets at the pre-defined timeframe" to "getting SDP installed with a longer term roadmap".

e) A previous investigation [APP5] suggested a compute node to be made up of one CPU and three GPU devices for executing 3 instances of the same pipeline. This suggestion was meant to optimise capital spend, real estate space, and operating wattage consumption. However, memory availability and scaling issues will affect the number of instances supported per compute node for conflicting effects. This type of architectural design issues exists. They pose more uncertainty than the hardware landscape and should be addressed immediately.

Appendices

APP1- Summary of Investigation Report TSK-1707

a) COTS and Open Standard as Policy: It is a coincidence that this investigation took place in 2017 which marks the emergence of industry responses to the phenomenon of Moore Hitting the Wall. Some responses are marketed as closed source solutions and others are proposed as open standard. SDP has expressed the desire for Commercial off the Shelf (COTS) solutions. COTS solutions are not necessarily the most powerful or power efficient but would have the best price performance and presumably the widest level of operation and maintenance support. This study has expressed comfort in this direction.

b) Hardware Technology Readiness: Assuming that the main SDP hardware procurement contract will start full delivery in 2024 which is 7 years away from the time of writing (2017-08), it is highly likely that SDP will be in time to get the benefits of major upgrades of x86 technologies to the extent of meeting previously expressed hardware targets.

c) Contributions to SDP Design: In addition to the estimation that hardware technologies would be ready for SDP by 2024 in terms of performance and power efficiency subject to the acceptance of single precision for SDP domain applications, the following list would assist compute node design in the period leading to full delivery.

- The idea of caching of memory and storage for meeting domain application requirements could be applied to compute node and compute island designs.
- Use of memory resource for application data will not be 100% of the installed capacity. This warning must be observed until more specific utilisation ratio is known.
- SSD has a Terabyte Write (TBW) limit. This warning must be observed by estimating the 'volume of data write' to get an idea of the physical longevity of SSD.
- The release and industry support of PCIe Gen 4, OpenCAPI and/or GEN-Z within the next few years would have a wide scope positive spin on compute node and compute island designs.

APP2- Summary of Investigation Report TSK-1808

a) This exercise revealed the critical role of main memory size as it imposed restrictions on how much computation a compute node can do well before the issue of memory access bottleneck is reached. Obviously a bigger grid shape is wanted and this is the first challenge to resolve. For 64GB of installed compute node main memory, the biggest grid computable found in this investigation for Multi-Frequency Synthesis was [8, 1, 8192, 8192] where 8 refers to the number of frequency channels and 1 refers to the number of polarisations. Image grids took 28GB, UV grids in complex took 8GB, visibilities and miscellaneous data were allocated 1GB, the operating system and associated services were allocated 3GB, leaving an estimated 24GB for runtime buffering. Double Precision (64b) was the default of Python, and a request to do Single Precision (32b) was not accepted by Python.

b) Apart from the grid shape, this investigation settled on (166x165/2) baselines. Variation of test parameters was limited to the number of major cycles (1 and 5), number of minor cycles (1 and 100), number of time steps (10 and 200), and unexpectedly the footprint of the point spread function for deconvolution (8192 and 200). Figures in brackets were the scenarios tested.

c) The collective runtime of the five chosen algorithms was found to be quite low (61% for the test parameters tested) and the original plan of verifying the heuristic model on arithmetic intensity and hardware utilisation of the pipeline was not pursued.

d) The other 39% of the runtime of the continuum imaging pipeline tested was used by coalescing and de-coalescing of visibility data and mapping functions for pipeline computations. We did not expect these activities to be as significant as 39%. They are supporting activities of the pipeline and not the mission in their own right. Deconvolution is certainly the most important function of this mission along with gridding and Fourier transforms.

e) This investigation revealed the dominance of Deconvolution which is a dominant algorithm for reaching SDP dynamic range targets. Fast Fourier Transforms were found to have low dominance as the number of transforms did not increase for higher numbers of time steps as written in ARL. Gridding and De-gridding were dominant. Various scenarios tested suggested the above to be the subject matters for balancing (sweet spot finding) towards SKA high priority science objectives.

f) Runtime was analysed for dominant algorithms in the pipeline and not in terms of the arithmetic intensity, hardware utilisation, or the estimation of SDP size. This is because ARL was written in Python- an interpreter which was great for clarity and revision flexibility but poor for computational performance. Potential next steps were to investigate if GPU or APU would do better than CPU.

g) Obviously time steps and frequency channels can be processed in parallel across multiple nodes for the entire pipeline. They can be seen as the second level of parallelization if the intended purpose of this investigation based on the implication of Amdahl's Law is the first level.

APP3- Summary of Investigation Report TSK-2105

a) Hardware Landscape: Selection of the best processors and hardware for SDP will get harder over time due to architectural divergence of vendor products as a consequence of the slowing down of Moore's Law and its subsequent demise in the not-too-distant future.

b) Single Precision: The merits of running science pipelines in single precision (SP) in the GPU are significant. SP allows a bigger problem size such as the grid size or more Taylor terms to be accommodated in the limited GPU memory. There is also a slight increase of computation performance in SP over DP as far as the GPU is concerned [APP5]. Capital price and wattage consumption are beneficiaries as well. The same merits may not be applicable to CPU so the serial portions of science pipelines can continue to run in double precision in the CPU. Supporting these claims are efforts of testing parallel computing tools in the python ecosystem such as pyCUDA.

c) Co-Design: This investigation took a compute node perspective and is essentially a co-design effort. This investigation has identified four recommendations for SDP attention.

1. The Algorithm Reference Library should be ready
2. Algorithm design choices should be made that will affect the computation workload or complexity noting that design choices may change when algorithms change
3. Algorithms shall be optimized for performance to the point without restricting to one specific commercial hardware device
4. Costs of global synchronization blocks and scaling shall be revealed

APP4- Summary of Investigation Report TSK-2271

a) The first obstacle encountered in this investigation was that this series of APU was not officially supported by AMD for Linux operating systems as of 2018-04 as indicated by an Ubuntu user web forum: https://askubuntu.com/questions/1007350/what-is-needed-to-use-raven-ridge-ryzen-5-2400g. The forum suggested going for Ubuntu 18.04 Beta 2 and Linux kernel 4.16-rc3 with Padoka PPA, applying MESA 18.0 or 18.1 against LLVM 5.0 or 60 AMDGPU backend for Vega support. All these software packages were work in progress as of 2018-04-13. Also nothing online mentioned any success of the iGPU running on OpenCL. In the meantime (2018-04-27), the investigation managed to get the APU running under Windows 10 and the unofficial versions of Ubuntu in order to obtain some interim findings.

b) In the meantime the integrated GPU of the APU, when running OpenCL 1.1 under Ubuntu beta, was found to be marginally faster than the discrete GTX1050Ti card running CUDA 9 on FFT. This finding was motivating as the iGPU has less number of cores than the discrete GPU.

c) The full data set dimensions have been proven to be not an obstacle for the APU-OpenCL pair with a total of 64GB of memory (whereas CUDA GPU 4GB failed). This is the 2nd motivating finding. It is worth noting that the OpenCL runtime file was a generic version and was not obtained from AMD Radeon Open Compute platform (ROCm) which was the equivalence of CUDA to Nvidia.

APP5- Summary of Investigation Reports TSK-2395

a) Mission Achieved. This investigation proposed a model for estimating the required computational hardware size of SDP for executing a set of pre-defined pipelines. The model estimated the Composite Operational Intensity of a pipeline from its component algorithms, located the Roofline Efficiency of the pipeline running in a specific hardware device, applied the Programming Efficiency of the Oxford team, and finally obtained the Compute Efficiency of the device for the pipeline.

b) Contributions

1. Proposed an intuitive formula for working out the Composite Operational Intensity of a pipeline with a much higher level of certainty than using arithmetic, geometric, or harmonic mean of the component algorithms.
2. Incorporated Oxford Vertical Prototyping efforts into the context of the model and re-defined the term Compute Efficiency as the product of Programming Efficiency and a new term coined Roofline Efficiency.
3. Provided the interpretation that the Oxford vertical prototyping team achieved 55% DP compute efficiency for the Predict algorithms (consisting of Gridding and FFT) on Tesla P100 GPU and 65% DP on Titan-V GPU. Oxford Report Optimise_Predict_Step_algorithm.pdf. Both occasions are well above the current SDP estimate of 10%. Ref: Optimise_Predict_Step_algorithm.pdf and discussion notes: https://jira.ska-sdp.org/browse/TSK-1895.
4. Proposed a 'Single CPU Multiple GPU' compute node configuration to improve SDP runtime performance and to reduce capital price, rack space, and operating wattage consumption.

Field Code Changed

Field Code Changed

c) Bases and Assumptions

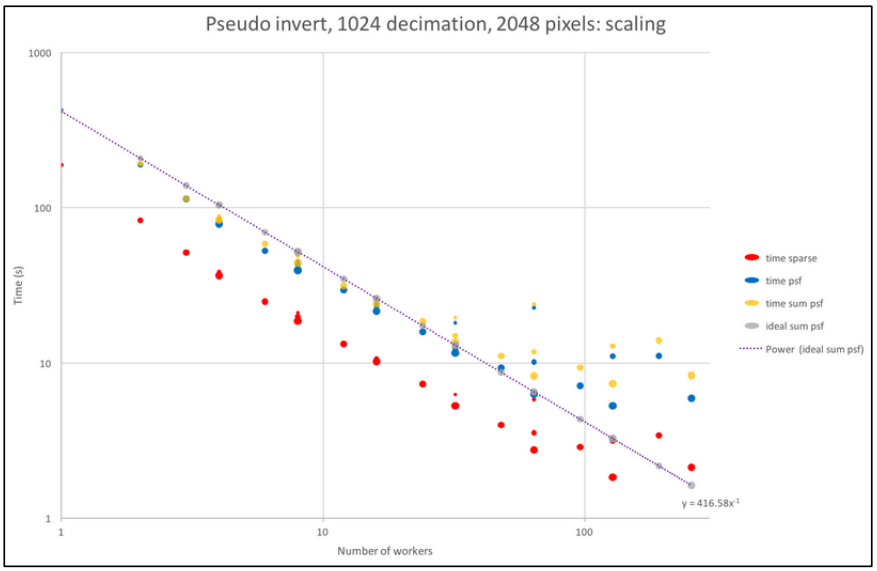
1. Concepts expressed by the Roofline model were faithfully observed
2. The standard x86 Acceleration model was applied. The CPU-only scenario has not been investigated due to the belief that the low computational capability of CPU will not satisfy SDP applications economically and perhaps technically due to scaling issues.
3. The source code from SDP ARL for the Test Continuum Imaging Pipeline was used for estimating the proportion of runtime taken by each parallel computing algorithm. Computation was single threaded as written in python and data arrays were handled with numpy.
4. The same source code was converted with pyCUDA and pyOpenCL for assessing the Operation Intensity of each major algorithm.
5. Oxford expertise of optimising parallel algorithms for GPU execution was used for estimating programming efficiency noting that Oxford did not use SDP ARL.
6. Algorithms of the Continuum Imaging Pipeline considered were FFT, Gridding, and MSMFS Deconvolution. Algorithms not considered included kernel generation, phase rotation, w-snapshots, and faceting. Other pipelines were not examined in this investigation but the methodology should remain applicable.
7. A single compute node was used for executing the entire pipeline

APP6- Notes on Previous ARL Cluster Scaling Tests

a) Tim Cornwell has performed a lot of scaling tests in 2017-11 timeframe with Dask as the scheduler and various hardware platforms including his laptop, Darwin cluster and the official SDP Alaska. Tim created a simple algorithm for gridding and inverse FFT to obtain a mock PSF and to sum the PSF from workers together. Source: https://confluence.ska-sdp.org/pages/viewpage.action?pageId=235700447. Tim commented:

- Here is the best scaling curve. The size of the markers represents the number of nodes used (ranging between 1 and 4).
- The efficiency (measured as scaled time divided by the actual measured time) shows a drop to about 40% for 128 workers. Fitting these 2 figures to Gunther's scaling expression gave b = 9E-5 or close to x = 4. This is a serious sub-scaling situation.

b) More threatening is the phenomenon of negative scaling with more than 100 nodes. Negative scaling refers to the state when an additional worker to the compute cluster reduces overall productivity. This is a fatal scenario for mitigation.



End of Memo